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Avalanche Behavior of Power MOSFETs

INTRODUCTION

Today, most DC-DC power supplies for industrial servers and telecommunication base stations as well as in automotive applications feature Power MOSFETs. In order to increase efficiency the need for the development of devices that combine low on-state resistance and low switching losses becomes apparent. In addition, the devices need to show excellent reverse-recovery behavior and high avalanche ruggedness, the latter being examined in this work. All measurements and simulations were performed employing Infineon's new OptiMOS®2 transistor and technology [1].

THEORY

During an avalanche event (impact ionization), the present high electric field accelerates an electron. The electron moves through the crystall and may collide with an lattice atom thus creating an electron-hole pair. If many electrons are subject to such collisions it is called an avalanche process. It can also be regarded as inverse Auger process [2]. Several models describing the impact ionization process have been developed, for example [3,4,5] but a discussion of those is not in the scope of this work. We merely state that we use the Valdinoci model [6,7], since it delivers better temperature dependence of breakdown voltage as the standard Chynoweth model [8] using the parameters obtained by van Overstraeten and de Man [9].
Another important parameter is the intrinsic carrier concentration. It strongly depends on temperature and can be approximated by the following empirical formula [10]:

$$n_i(T) = 3.88 \cdot 10^{16} \cdot T^{\frac{3}{2}} \cdot \exp(-\frac{7000K}{T}) \cdot cm^{-3} \quad (1)$$

By means of this formula and knowledge of the background doping it is possible to calculate the intrinsic temperature at which n_i reaches the background doping.

FAILURE MECHANISMS

The first mechanism is related to the self-heating of the device. Obviously, the lattice temperature increases due to the presence of high electric field and high current density as decribed by the heating term: $\frac{P_{th}}{V} = \vec{E} \cdot \vec{J}$. The breakdown voltage rises due to high current and increased carrier-phonon interaction. The temperature continues to rise until it gets in the vicinity of the so-called intrinsic temperature [11]. At this point, the device is not able to dissipate more energy thus if the current continues it will be destructed due to too high a temperature.

The second mechanism that results in the destruction of MOSFET devices is called non-thermal destruction, and is related to the turn-on (latch-up) of the parasitic npn-transistor. The holes generated by impact ionization flow through the p-Body region of the n-channel MOSFET thus creating a potential drop in the base region of the parasitic bipolar transistor. If this potential drop exceeds the built-in potential of the base-emitter diode the parasitic BJT will turn-on, i.e. latch-up. Since a BJT has a negative temperature coefficient of breakdown voltage latch-up is self-amplifying, while in case of avalanche, a uniform current distribution is supported by the positive temperature coefficient of the breakdown voltage. [12,13]

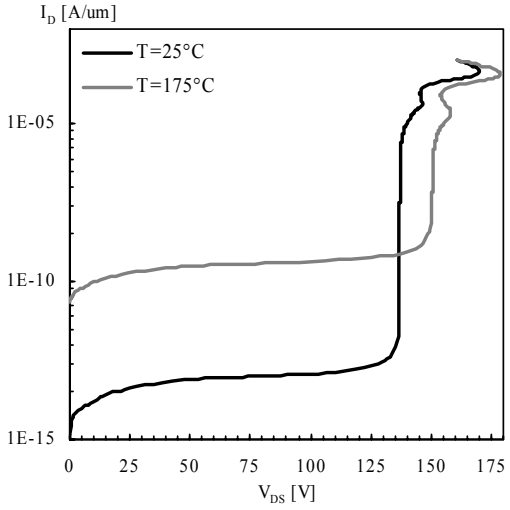

Fig. 1: simulated breakdown characteristics of transistor for T=25°C and T=175°C

Another possible destructive mechanism could be the snapback of breakdown voltage if the drain current exceeds a certain limit. The breakdown characteristics for two different temperatures can be seen in Fig. 1. A region with negative differential resistance does exist and causes the voltage to snap back. The reason for this snapback effect lies in the second breakdown of the MOSFET.

TEST SETUP AND FAILURE MODE

In certain applications a failure mode called unclamped inductive switching (UIS) can occur. The aim of the UIS test is to determine the maximum avalanche current the device is able to sustain. To this purpose, a circuit as depicted in Fig. 2 can be used.

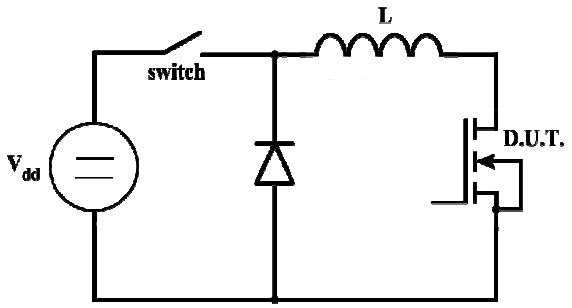

Fig. 2: principle circuit to determine the unclamped inductive switching behavior of a transistor. The voltage source is disconnected when the transistor turns off.

It consists of a voltage source, an external switch, a freewheeling diode, an inductance and the device under test (D.U.T.). While the transistor is turned on ($V_{GS} = 20V$) and the external switch is closed, the current ramps up according mainly to the inductance and the applied voltage. After turning off the device (and at the same time disconnecting the voltage source), the energy stored in the inductance must be dissipated in the transistor. Since the current continues to flow through the inductance the transistor is forced to maintain the current. Thus it is driven into avalanche mode.

The ramping process is iterated for a higher current until the device fails. By repeating this process with different inductances the UIS behavior can be well characterized in particular the dependence of maximum current I_{as} on inductance in the circuit. A typical example for thermal destruction is shown in Fig. 3.

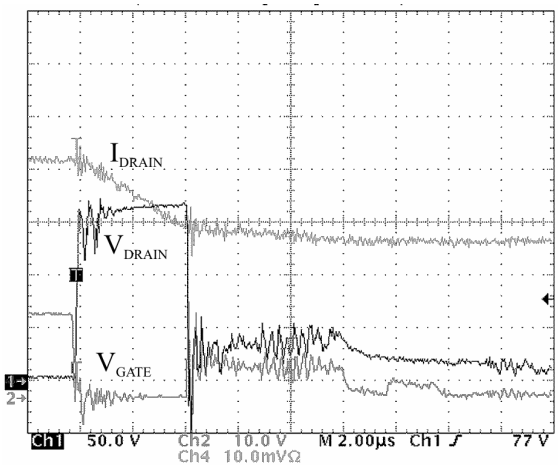

Fig 3: UIS measurement at large inductance clearly showing thermal destruction

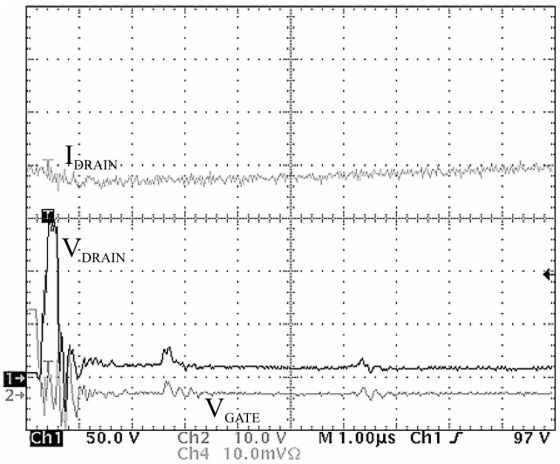

Fig. 4: UIS measurement indicating non-thermal destruction

The short transient time (<<1µs) until the device is destroyed indicates a different mechanism than thermal destruction as outlined in the last section. Fig. 4 depicts a non-thermal destruction behavior of a device. A rather broad distribution of measured I_{as} is characteristic for this mechanism.

SIMULATION RESULTS

To simulate the UIS behavior of the devices, several methods can be used. For thermal destruction, single cell simulations proved feasible and sufficient. The so-called intrinsic temperature can be estimated from measurements as well as evaluating the dependence of intrinsic carrier concentration n_i over temperature. An intrinsic temperature of 380°C could be extracted by means of eq. 1.

Good agreement between simulation and measurement was obtained for the thermal destruction, that is for larger inductances as depicted in Fig. 5. For smaller inductances the different destruction mode is clearly observable. The transition in measurement occurs approximately at an inductance of $L \approx 100\mu H$.

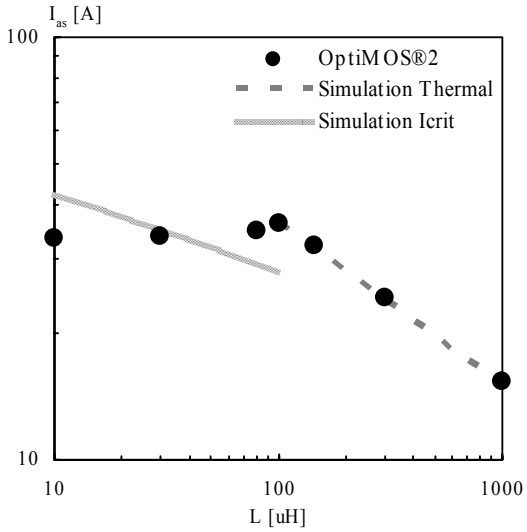

Fig. 5: comparison between measurement (dots) and simulation (grey, dashed) of maximum avalanche current vs. inductance at room temperature. Note the kink in the measured curves indicating the transition from thermal destruction to non-thermal destruction

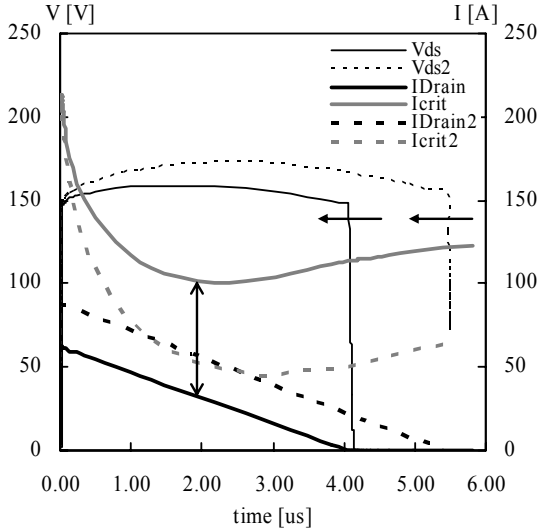

Fig. 6. simulated UIS behavior for two different currents I_{Drain} (solid lines) and I_{Drain2} (dashed lines). At I_{Drain} a significant gap between I_{Drain} and I_{crit} exists (arrow), whereas at I_{Drain2} this gap vanishes indicating destruction (I_{Drain2}>I_{crit2})

The thermal behavior can roughly be estimated if the one-dimensional heat transport equation and some other simplifications are applied to the device. Beside other dependencies, the maximum sustained avalanche current I_{as} and the inductance L are related: $I_{as} \propto L^{-\frac{1}{3}}$. The measurement reveals a little bit smaller exponent (~-0.39). However, the two curves show sufficient agreement between experiment and simulation.

A more exact analysis needs to take into account for example device dimensions [14]. To simulate the UIS behavior in the non-thermal destruction regime we use the static isothermal simulation of the breakdown and identify a critical current for different temperatures. If, for example, the critical current was defined as the point at which the device enters the region of negative differential resistance a criterion for non-thermal destruction is derived. I_{crit} changes with temperature as can be seen in Fig. 1. Including this temperature dependence into transient simulation as depicted in Fig. 6 the maximum sustainable I_{as} can be approximated. The simulation and measurement differ significantly from each other for small inductances as can be seen in Fig. 5. One possible reason is the different temperature distribution in case of transient simulation compared to static isothermal breakdown simulations. Furthermore, the possibility of current constriction to small regions of the device is thus far neglected.

CONCLUSION

The avalanche behavior of the new OptiMOS®2 transistor was investigated both experimentally and by means of simulation.

The avalanche current capability can be divided into two distinct regions in which several different destruction mechanisms affect the device's behavior. For large inductances thermal destruction dominates while for smaller inductances latch-up and field effects play a significant role.

The simulation of thermal destruction delivers quite good agreement to measurements. On the other hand, further work has to be done to get better results for simulation of non-thermal effects including simulation of further current constriction during an avalanche event.

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